AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for fabricating a semiconductor device, comprising the steps of:

(a) forming a semiconductor substrate structure including a substrate~~, a nitride layer for forming a hard mask~~, a plurality of conductive patterns, an etch stop layer, an inter-layer insulation layer, a nitride layer on top of the inter-layer insulation layer for forming a hard mask, an anti-reflective coating (ARC) layer and a photoresist pattern;

(b) selectively etching the ARC layer and the nitride layer with use of the photoresist pattern as ~~an~~ a first etch mask ~~to form a hard mask~~;

(c) removing the photoresist pattern and the ARC layer;

(d) etching the inter-layer insulation layer disposed between the conductive patterns by using the hard mask as an etch mask to form a contact hole exposing the etch stop layer;

(e) removing the etch stop layer formed at a bottom area of the contact hole to expose the substrate; and

(f) forming a plug electrically contacted to the exposed substrate, wherein the steps (b) and (d) to (e) proceeds in an in situ condition.

2. (Currently Amended) The method as recited in claim 1, wherein each of the conductive patterns has a stack structure including a hard mask insulation layer and a conductive layer.

3. (Original) The method as recited in claim 1, wherein at the step (e), the etch stop layer is removed by employing a blanket etching process or a cell open mask.

4. (Currently Amended) The method as recited in claim ~~1~~2, wherein the nitride layer is deposited with a predetermined thickness equal to or greater than the total thickness of lost portions of the hard mask insulation layer during the step (d) and the step (e).

5. (Original) The method as recited in claim 1, wherein at the step (e), the hard mask is simultaneously removed.

6. (Original) The method as recited in claim 1, wherein the inter-layer insulation layer is made of an oxide-based material and is etched by performing a self-aligned contact (SAC) etching process.

7. (Currently Amended) The method as recited in claim ~~6~~1, wherein the SAC etching process proceeds by employing an etch gas such as C_4F_6 and C_5F_8.

8. (Original) The method as recited in claim 1, wherein the step (a) includes the steps of:

depositing the nitride layer on the substrate on which the plurality of conductive patterns, the etch stop layer and the inter-layer insulation layer are sequentially formed, the substrate classified into a cell region and a peripheral circuit region;

forming the anti-reflective coating (ARC) layer on the nitride layer; and

forming the photoresist pattern on the ARC layer through an ArF photolithography;

9. (Original) The method as recited in claim 1, wherein the step (f) includes the steps of:

forming a conductive material for forming the plug to make an electric contact to the exposed substrate;

performing an etch-back process to remove a partial portion of the conductive material to diminish a height difference between the cell region and the peripheral circuit region; and

performing a chemical mechanical polishing process to the conductive material until an upper part of each conductive pattern is exposed.

10. (Original) The method as recited in claim 9, wherein the step of forming the conductive material for forming the plug proceeds by depositing the conductive material on an entire surface of the substrate or growing the conductive material from the exposed substrate through a selective epitaxial growth (SEG) technique.

11. (Original) The method as recited in claim 1, wherein the photoresist pattern is formed in a line type or a hole type.

12. (Original) The method as recited in 1, wherein the conductive pattern is one of a gate electrode pattern, a bit line and a metal wire.

13. (Currently Amended) A method for fabricating a semiconductor device, comprising the steps of:

(a) forming a semiconductor substrate structure including a substrate~~, a nitride layer for forming a hard mask~~ a nitride layer on top of the inter-layer insulation layer for forming a hard mask, a plurality of conductive patterns, an etch stop layer, an inter-layer insulation layer, an anti-reflective coating (ARC) layer and a photoresist pattern;

(b) loading the resulting semiconductor substrate structure into an etching equipment having at least two chambers;

(c) selectively etching the ARC layer and the nitride layer with use of the photoresist pattern as ~~an~~ a first etch mask ~~to form a hard mask~~;

(d) removing the photoresist pattern and the ARC layer;

(e) etching the inter-layer insulation layer disposed between the conductive patterns by using the hard mask as ~~an~~ a second etch mask to form a contact hole exposing the etch stop layer;

(f) removing the etch stop layer formed at a bottom area of the contact hole to expose the substrate; and

(g) forming a plug electrically contacted to the exposed substrate, wherein the steps (c) and (e) to (f) proceeds in an in situ condition.

14. (Original) The method as recited in claim 13, wherein the steps (c) and (d) are performed at a first chamber and the steps (e) and (f) are performed at a second chamber.

15. (Currently Amended) The method as recited in claim 13, wherein each of the conductive patterns has a stack structure including a hard mask insulation layer and a conductive layer.

16. (Original) The method as recited in claim 13, wherein at the step (f), the etch stop layer is removed by employing a blanket etching process or a cell open mask.

17. (Currently Amended) The method as recited in claim ~~13~~ 15, wherein the nitride layer is deposited with a predetermined thickness equal to or greater than the total thickness of lost portions of the hard mask insulation layer during the step (e) and the step (f).

18. (Original) The method as recited in claim 13, wherein at the step (f), the hard mask is simultaneously removed.

19. (Original) The method as recited in claim 13, wherein the inter-layer insulation layer is made of an oxide-based material and is etched by performing a SAC etching process.

20. (Currently Amended) The method as recited in claim 19~~13~~, wherein the SAC etching process proceeds by employing an etch gas such as C_4F_6 and C_5F_8.

21. (Original) The method as recited in claim 13, wherein the step (a) includes the steps of:

depositing the nitride layer on the substrate on which the plurality of conductive patterns, the etch stop layer and the inter-layer insulation layer are sequentially formed, the substrate classified into a cell region and a peripheral circuit region;

forming the anti-reflective coating (ARC) layer on the nitride layer; and

forming the photoresist pattern on the ARC layer through an ArF photolithography;

22. (Original) The method as recited in claim 13, wherein the step (g) includes the steps of:

forming a conductive material for forming the plug to make an electric contact to the exposed substrate;

performing an etch-back process to remove a partial portion of the conductive material to diminish a height difference between the cell region and the peripheral circuit region; and

performing a chemical mechanical polishing process to the conductive material until an upper part of each conductive pattern is exposed.

23. (Original) The method as recited in claim 22, wherein the step of forming the conductive material for forming the plug proceeds by depositing the conductive material on an entire surface of the substrate or growing the conductive material from the exposed substrate through a SEG technique.

24. (Original) The method as recited in claim 13, wherein the photoresist pattern is formed in a line type or a hole type.

25. (Currently Amended) The method as recited in 13, ~~wherein~~ each of the conductive patterns is one of a gate electrode pattern, a bit line and a metal wire.